QPA1001

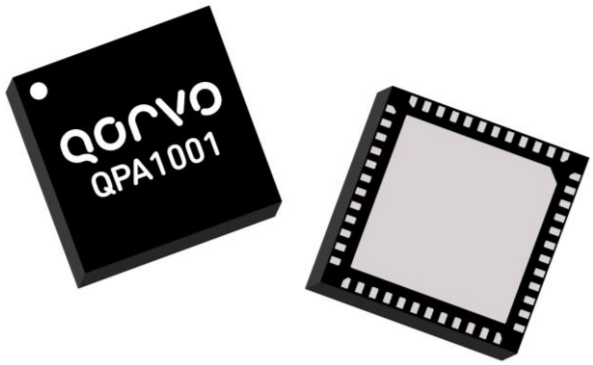
3.1 – 3.5 GHz 60 Watt GaN Power Amplifier

Product Description

Qorvo's QPA1001 is a high-power, S-band amplifier fabricated on Qorvo's QGaN25 0.25um GaN on SiC production process. Covering 3.1-3.5 GHz, the QPA1001 typically provides 48 dBm of saturated output power and 22 dB of large-signal gain while achieving 54 % power-added efficiency.

The QPA1001 can also support a variety of operating conditions to best support system requirements. With good thermal properties, it can support a range of bias voltages and will perform well under pulse applications. The QPA1001 is matched to 50 ohms with integrated DC blocking caps on both I/O ports. The QPA1001 utilizes a plastic QFN overmolded package, which is ideal for use in both commercial and military radar systems.

Lead-free and RoHS compliant.

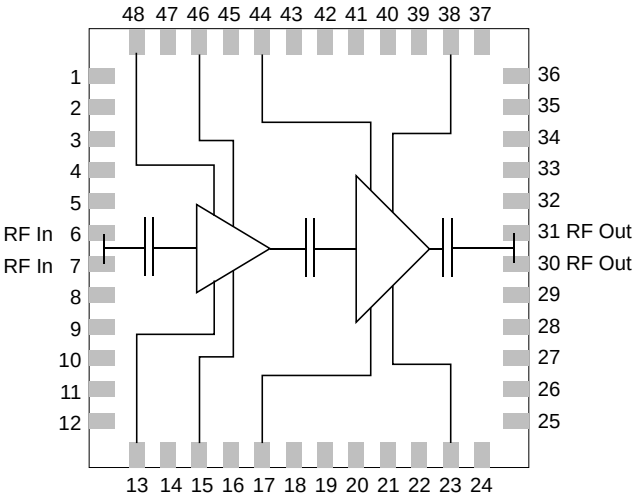


Product Features

- Frequency Range: 3.1 – 3.5 GHz
- Pout: 48 dBm (P_{IN} = 26 dBm, 3.3 GHz)
- Large Signal Gain: 22 dB (P_{IN} = 26 dBm)
- PAE: 54 % (P_{IN} = 26 dBm)
- Bias: V_D = 30 V, I_{DQ} = 200 mA
- Plastic Overmold QFN Package
- Package Dimensions: 7.0 x 7.0 x 0.85 mm

Performance is typical across frequency. Please reference electrical specification table and data plots for more details.

Functional Block Diagram



Applications

- Military Radar
- Commercial Radar

Ordering Information

Part	Description
QPA1001	3.1–3.5 GHz 60 W GaN Power Amplifier (10 pcs.)
QPA1001TR7	7" Reel – 500 pcs.
QPA1001EVB	QPA1001 Evaluation Board

Absolute Maximum Ratings

Parameter	Value / Range
Drain Voltage (V_D)	40 V
Drain Current (I_{D1}/I_{D2})	0.80/5.70 A
Gate Voltage Range	−6 to 1 V
Gate Current (I_G)	See I_G plot, pg. 10
Dissipated Power (P_{DISS})[1]	95 W
Input Power (V_D=30V, 50 Ω, 85 °C)	31 dBm
Input Power (4:1 VSWR, 85 °C)	28 dBm
Storage Temperature	−55 to 150 °C

Note:
[1] T_{BASE} = 85 °C

Operation of this device outside the parameter ranges given above may cause permanent damage. These are stress ratings only, and functional operation of the device at these conditions is not implied.

Recommended Operating Conditions

Parameter	Value
Drain Voltage (V_D)	30 V
Drain Current (quiescent, I_{DQ})	200 mA
Drain Current (under drive, I_D)	4.5 A
Gate Voltage Range (V_G)	−2.8 to −2.0 V
Operating Temperature Range	−40 to 85 °C

Electrical specifications are measured at specified test conditions. Specifications are not guaranteed over all recommended operating conditions.

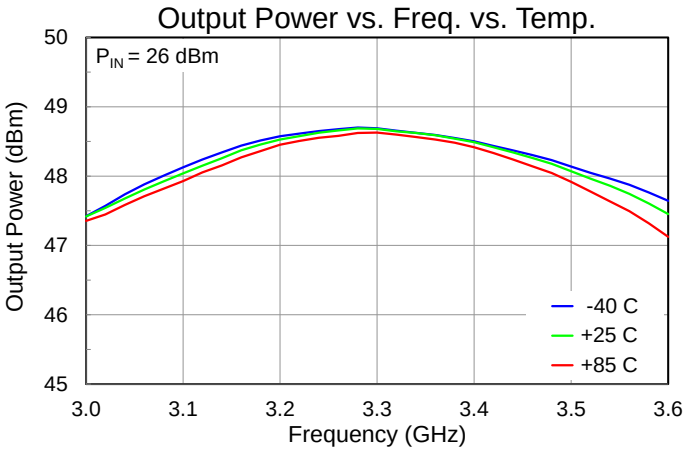
Electrical Specifications

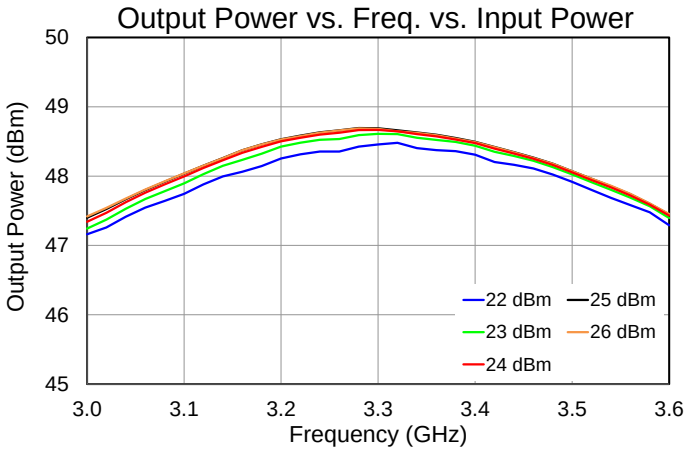
Test conditions, unless otherwise noted: 25 °C, V_D = 30 V, I_{DQ} = 200 mA, Pulse Width = 100 us, Duty Cycle = 10%

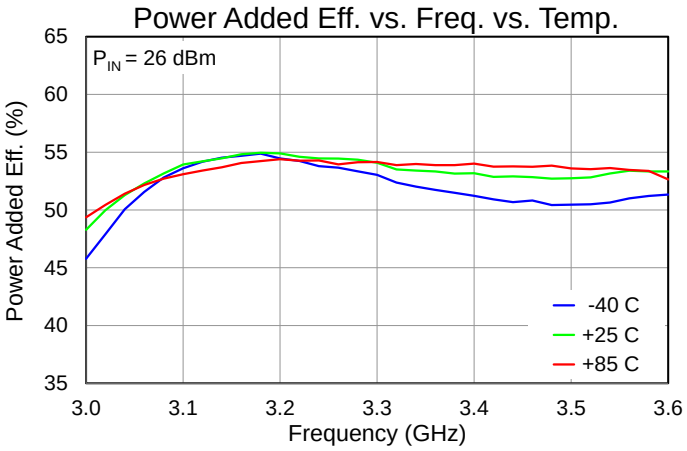
Parameter		Min	Typ	Max	Units
Operational Frequency Range		3.1	3.3	3.5	GHz
Output Power @ P_{IN} = 26 dBm	Frequency = 3.1 GHz		48.0		dBm
	Frequency = 3.3 GHz		48.7		
	Frequency = 3.5 GHz		48.0		
Power Added Efficiency @ P_{IN} = 26 dBm	Frequency = 3.1 GHz		53.9		%
	Frequency = 3.3 GHz		54.1		
	Frequency = 3.5 GHz		52.7		
Small Signal Gain	Frequency = 3.1 GHz		25.5		dB
	Frequency = 3.3 GHz		25.3		
	Frequency = 3.5 GHz		25.6		
Input Return Loss	Frequency = 3.1 GHz		16.3		dB
	Frequency = 3.3 GHz		12.5		
	Frequency = 3.5 GHz		10.4		
Output Return Loss	Frequency = 3.1 GHz		14.2		dB
	Frequency = 3.3 GHz		9.8		
	Frequency = 3.5 GHz		8.6		
Output Power Temperature Coefficient			−0.001		dBm/°C
Recommended Operating Drain Voltage			30		V

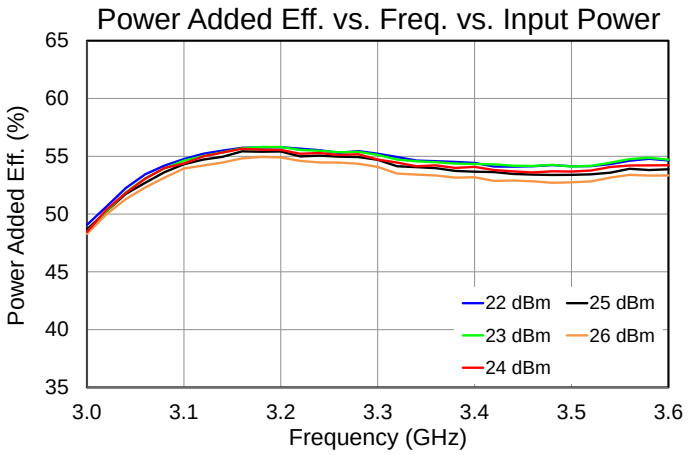
Performance Plots – Large Signal (Pulsed)

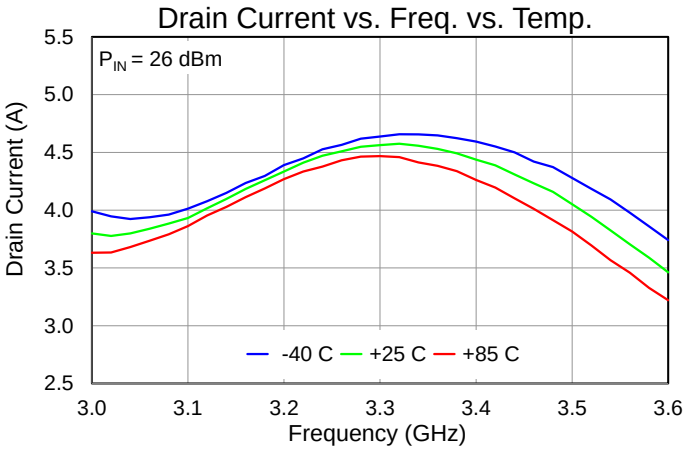
Test conditions unless otherwise noted: Temp. = 25 °C, V_D = 30 V, I_{DQ} = 200 mA, PW = 100 us, Duty Cycle = 10%

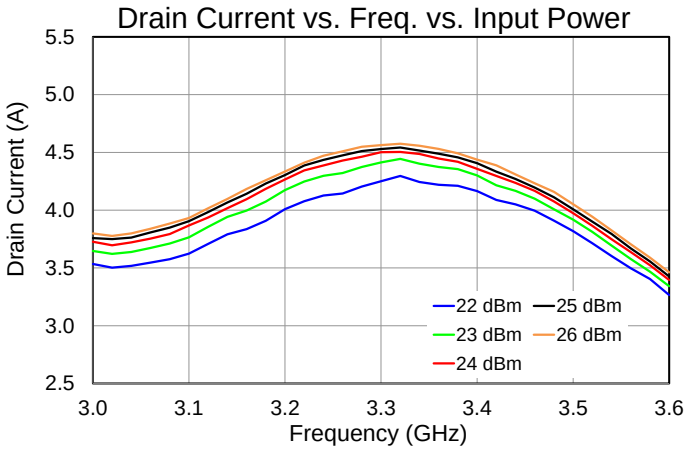












Performance Plots – Large Signal (Pulsed)

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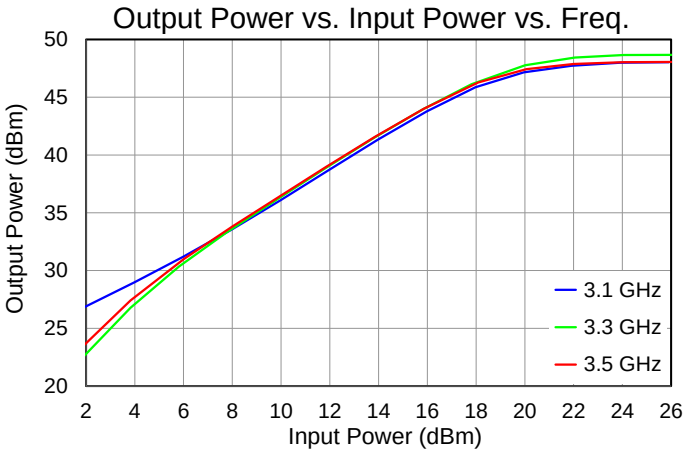
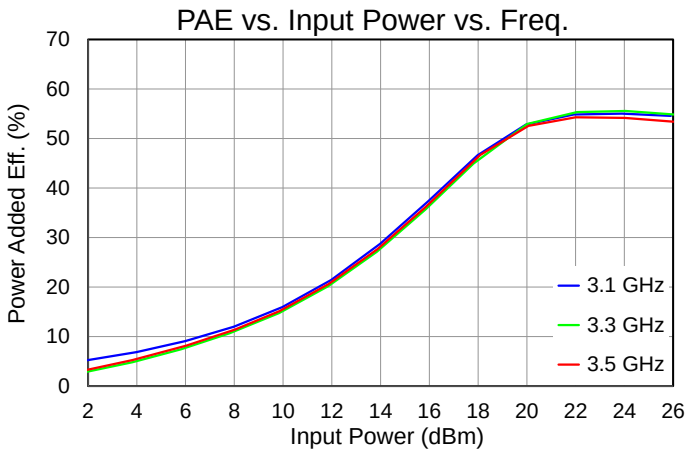
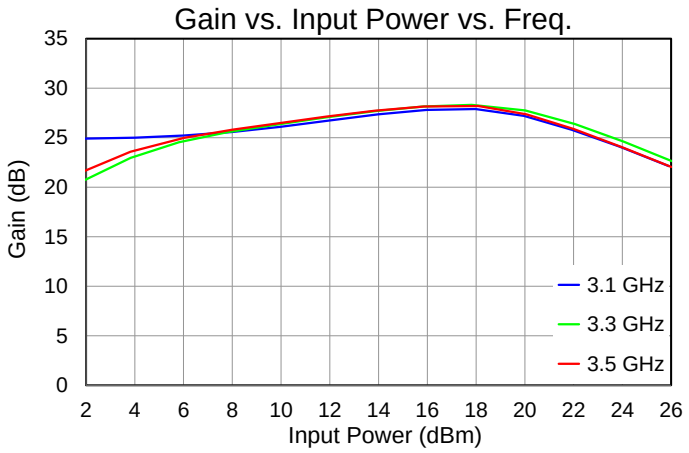
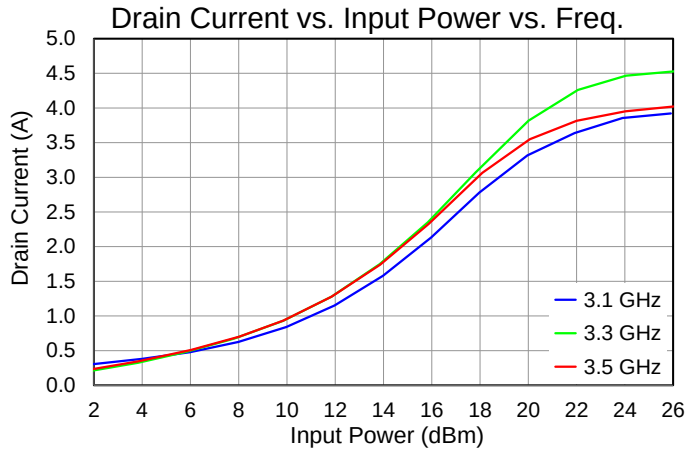
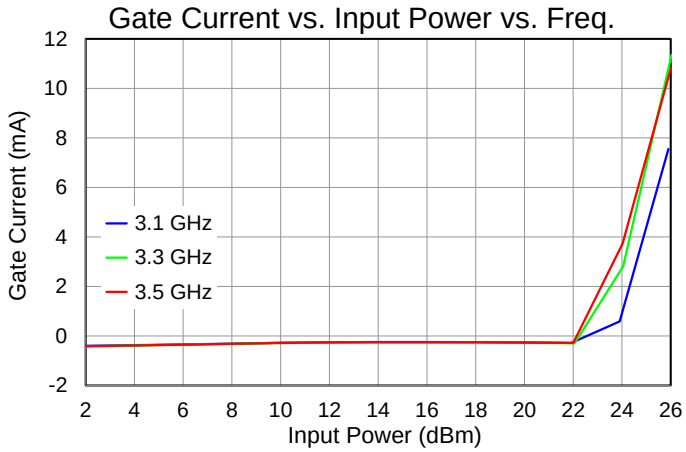




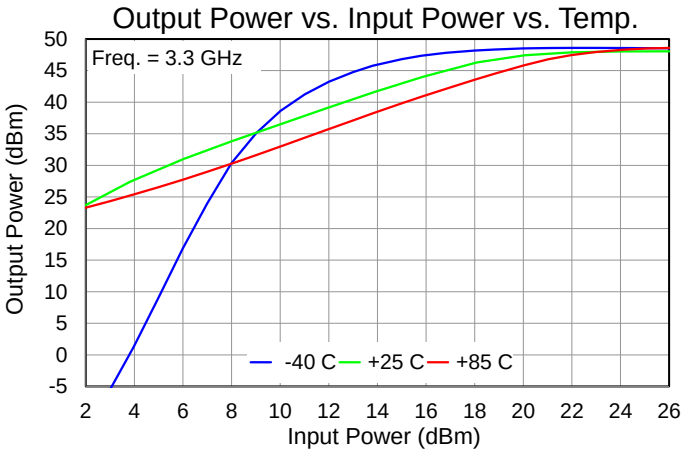


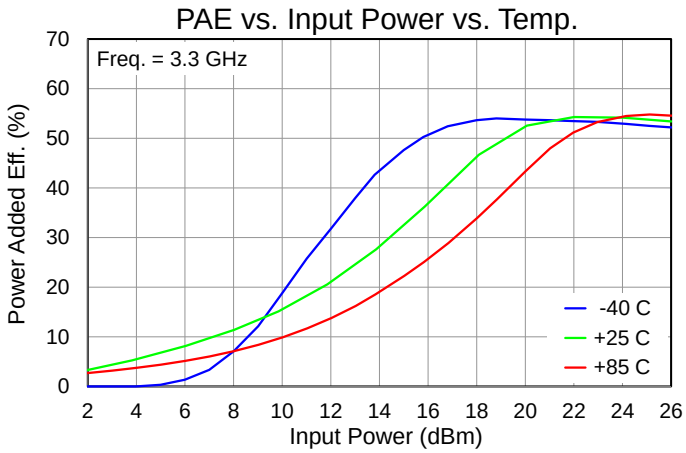


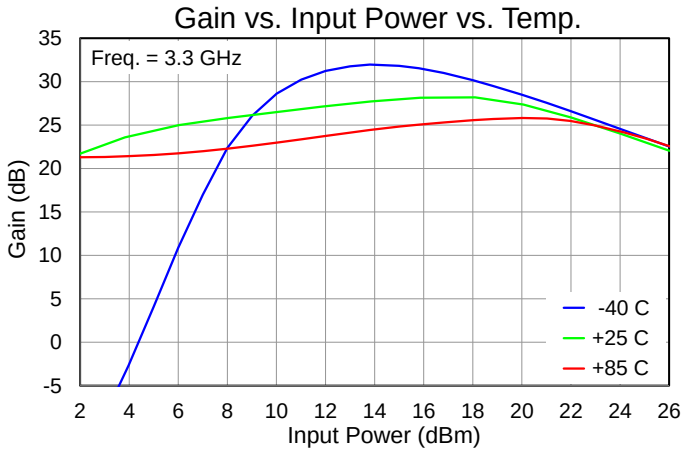


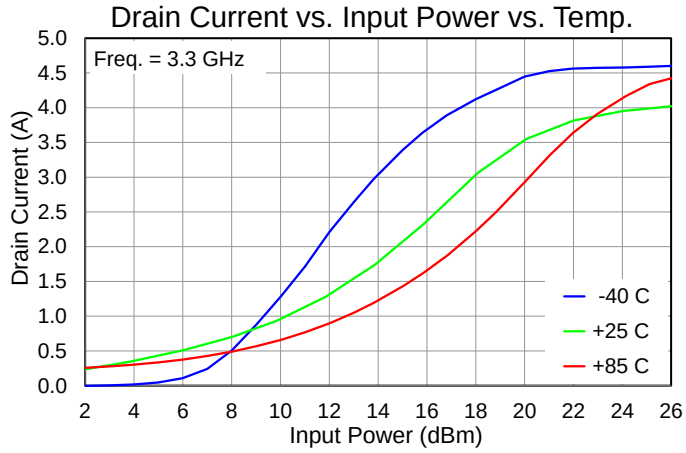
Performance Plots – Large Signal (Pulsed)

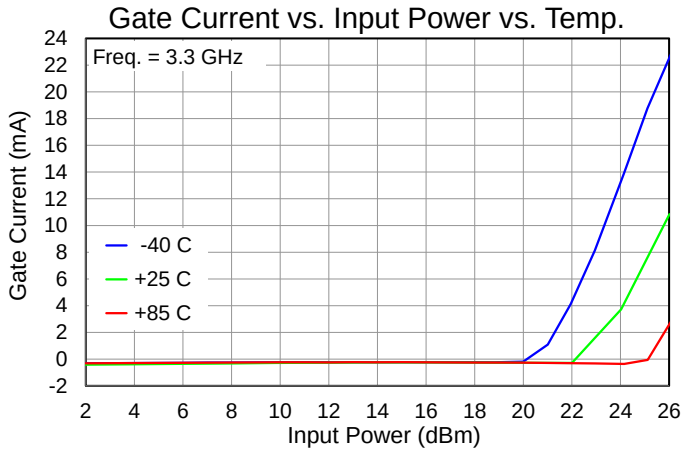
Test conditions unless otherwise noted: Temp. = 25 °C, V_D = 30 V, I_{DQ} = 200 mA, PW = 100 us, Duty Cycle = 10%





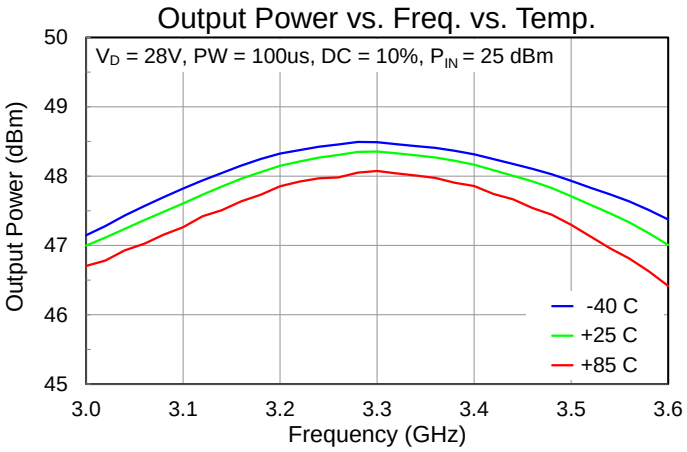


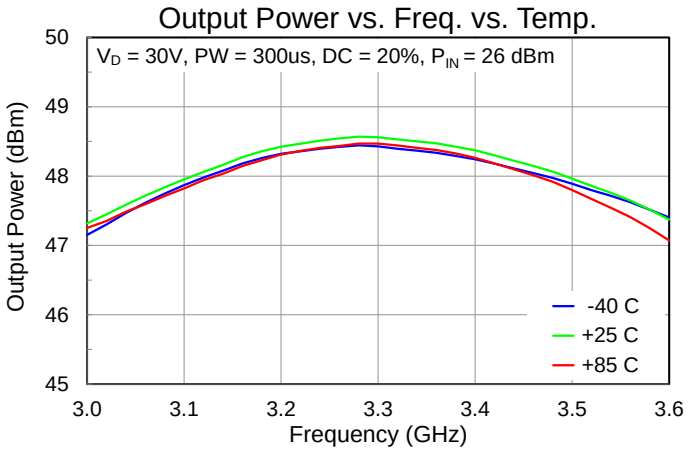


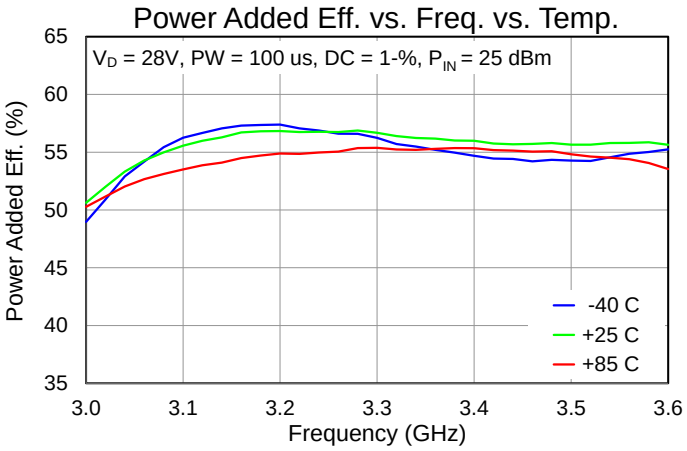


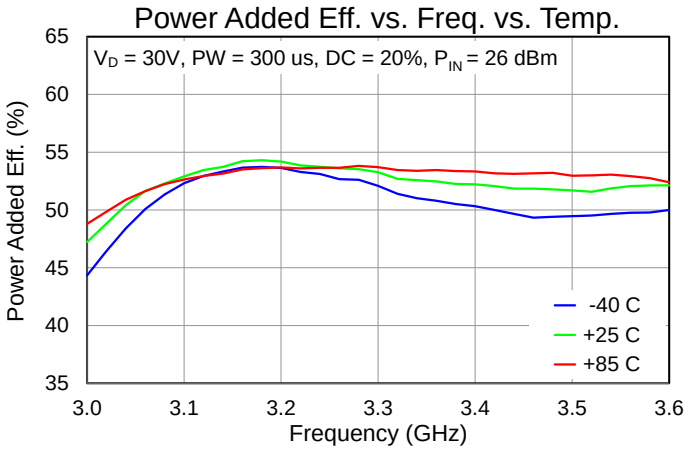
Performance Plots – Large Signal (Pulsed)

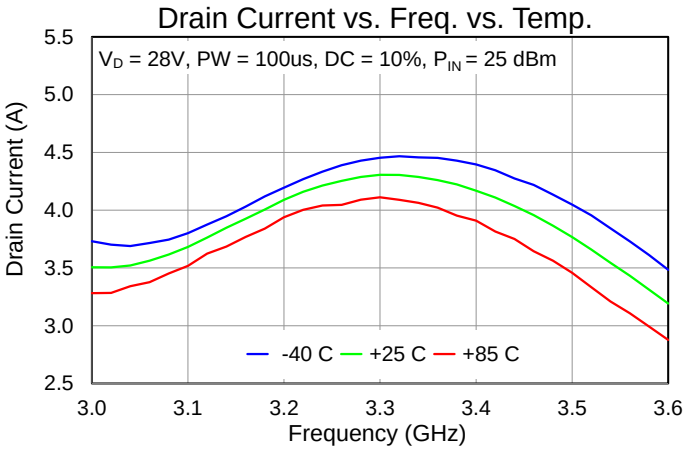
Test conditions unless otherwise noted: Temp. = 25 °C, I_{DQ} = 200 mA

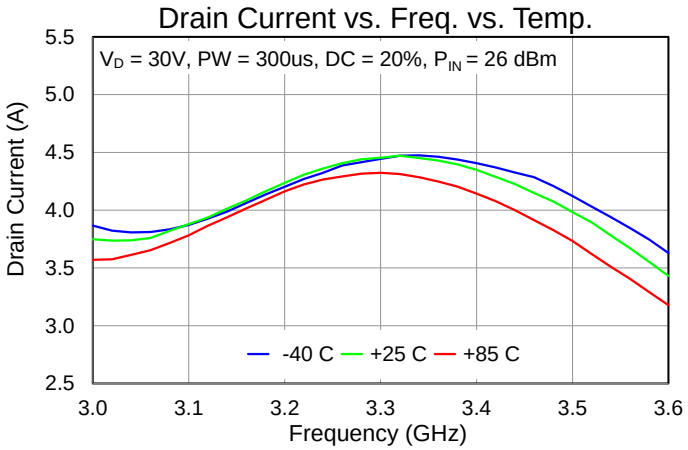








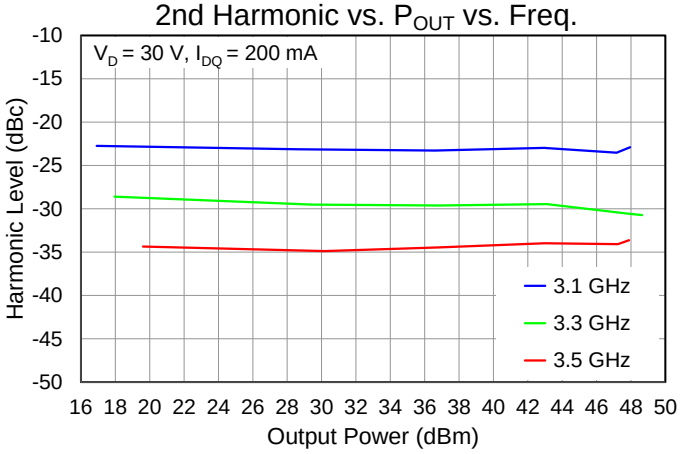




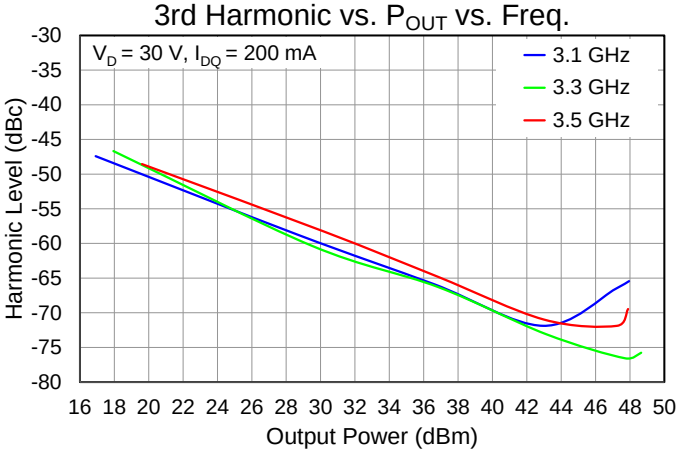
Performance Plots – Harmonics (Pulsed)

Test conditions unless otherwise noted: Temp. = 25 °C, PW = 100 us, Duty Cycle = 10%

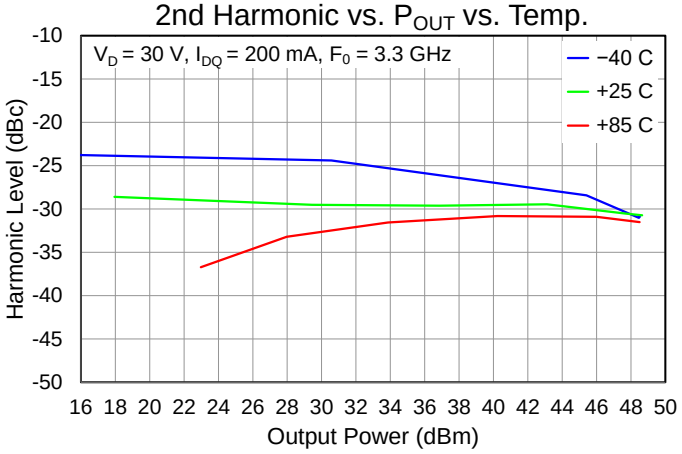
2nd Harmonic vs. P_{OUT} vs. Freq.



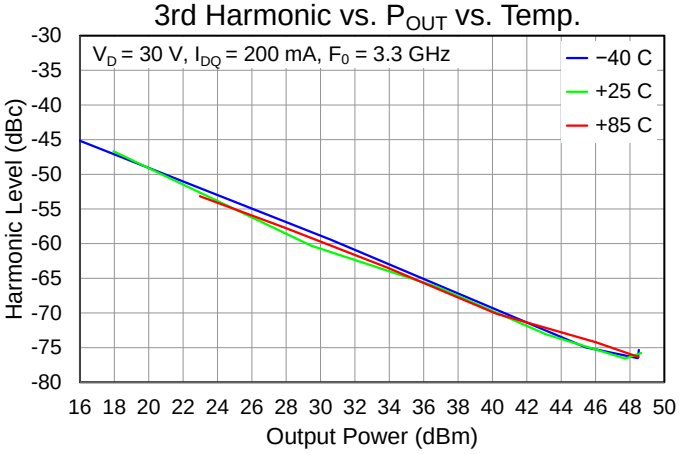
3rd Harmonic vs. P_{OUT} vs. Freq.



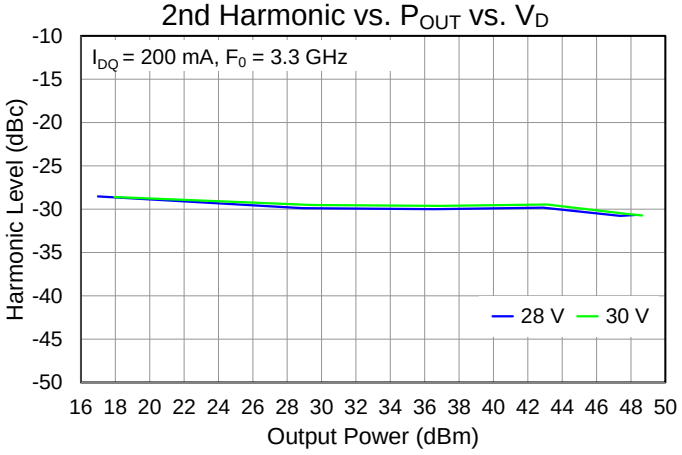
2nd Harmonic vs. P_{OUT} vs. Temp.



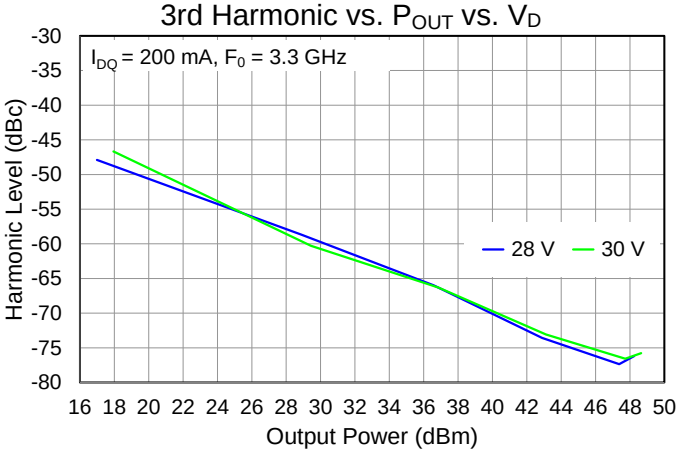
3rd Harmonic vs. P_{OUT} vs. Temp.



2nd Harmonic vs. P_{OUT} vs. V_D



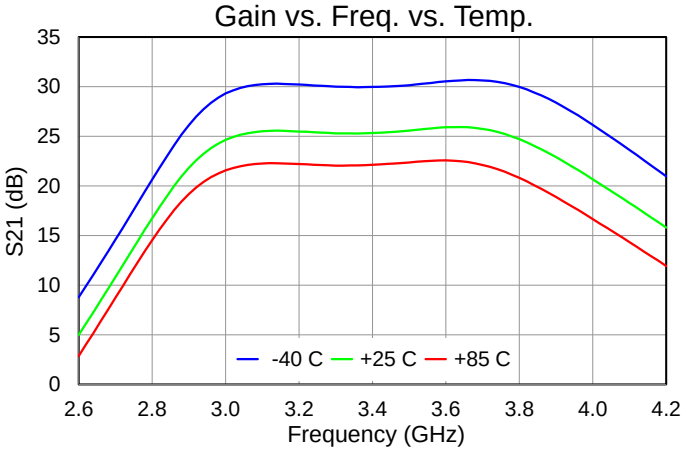
3rd Harmonic vs. P_{OUT} vs. V_D



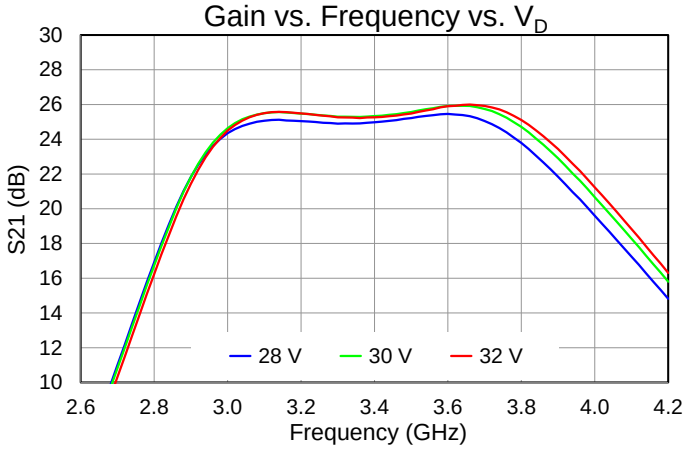
Performance Plots – Small Signal

Test conditions unless otherwise noted: Temp. = 25 °C, V_D = 30 V, I_{DQ} = 200 mA

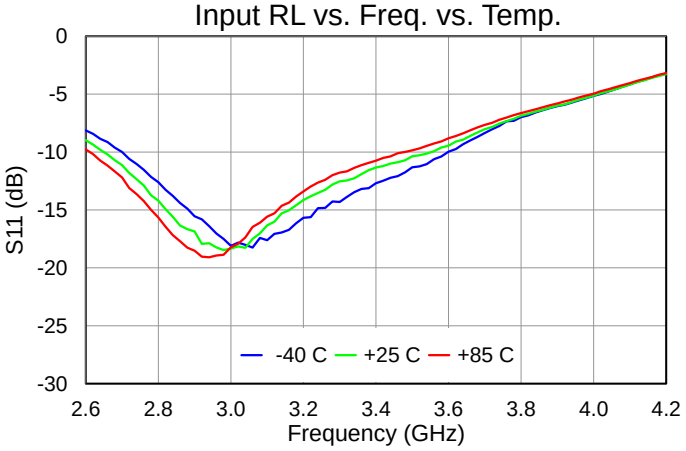
Gain vs. Freq. vs. Temp.



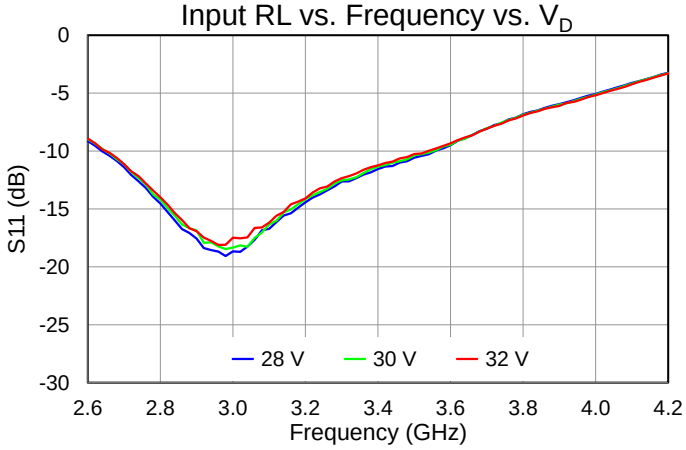
Gain vs. Frequency vs. V_D



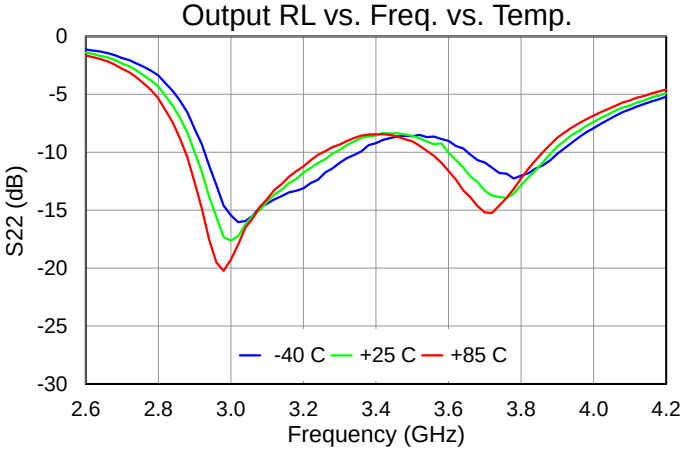
Input RL vs. Freq. vs. Temp.



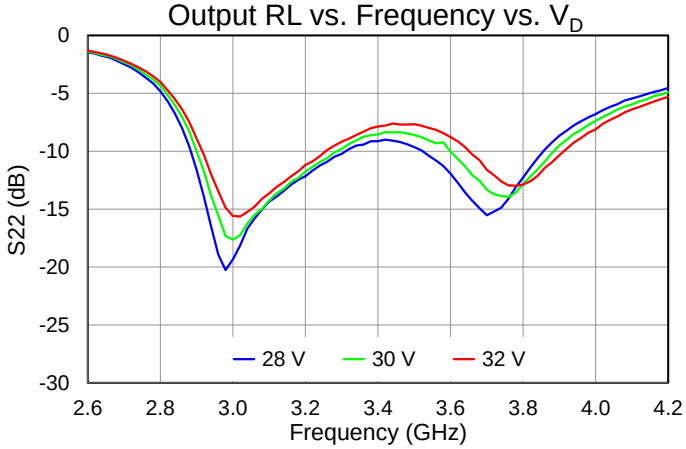
Input RL vs. Frequency vs. V_D



Output RL vs. Freq. vs. Temp.

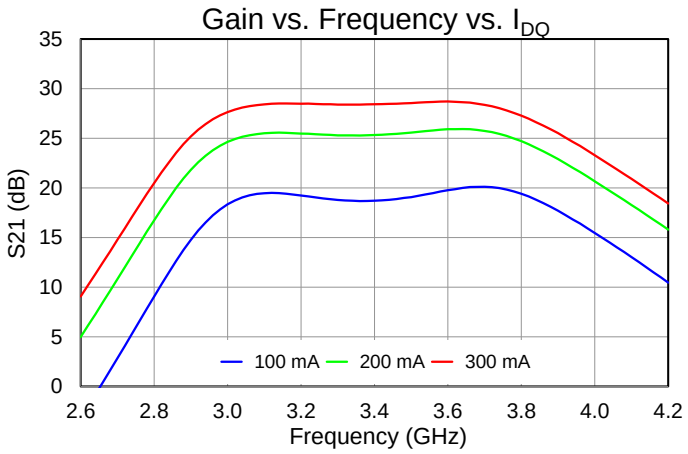


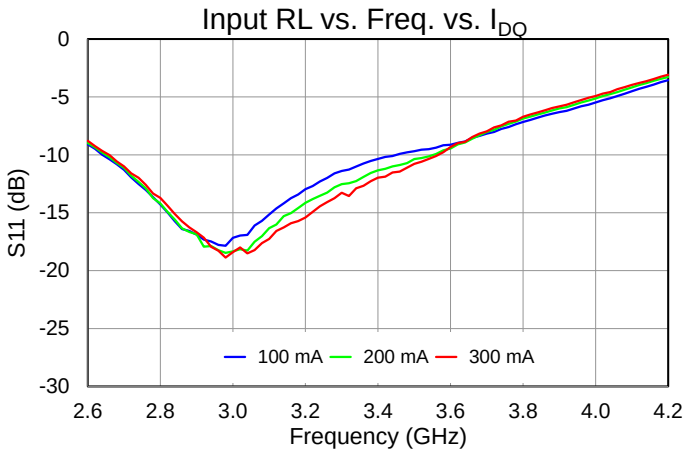
Output RL vs. Frequency vs. V_D

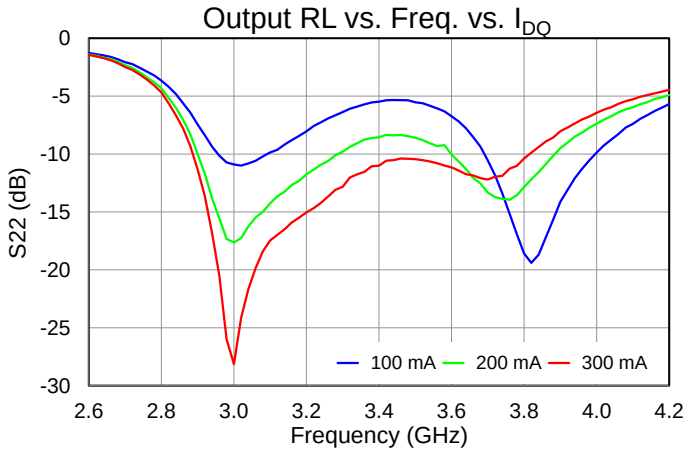


Performance Plots – Small Signal

Test conditions unless otherwise noted: Temp. = 25 °C, V_D = 30 V, I_{DQ} = 200 mA





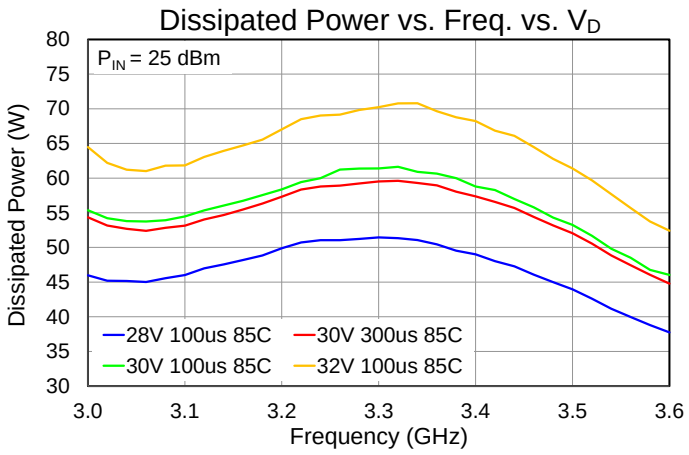


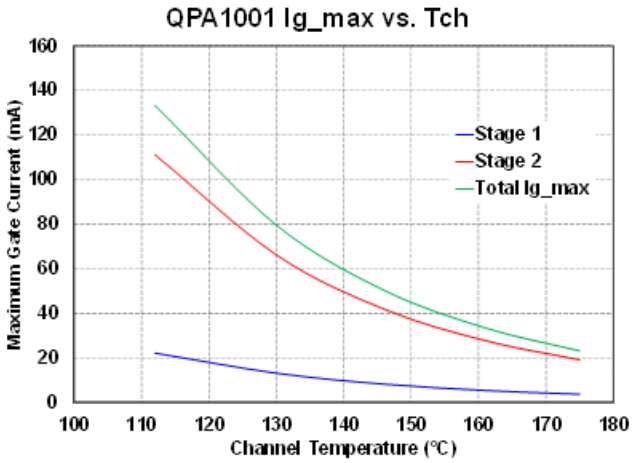
Thermal and Reliability Information

Parameter	Test Conditions	Value	Units
Thermal Resistance (θ_{JC}) (1)	T_{base} = 85°C, V_D = 30 V, I_{DQ} = 200 mA, Freq = 3.32 GHz, I_{D_Drive} = 4.46 A, P_{IN} = 26 dBm, P_{OUT} = 48.6 dBm, P_{DISS} = 61.6 W, PW = 100 us, DC = 10%	0.519	°C/W
Channel Temperature (T_{CH}) (Under RF drive)		117	°C
Thermal Resistance (θ_{JC}) (1)	T_{base} = 85°C, V_D = 30 V, I_{DQ} = 200 mA, Freq = 3.32 GHz, I_{D_Drive} = 4.31 A, P_{IN} = 26 dBm, P_{OUT} = 48.4 dBm, P_{DISS} = 60.5 W, PW = 300 us, DC = 20%	0.744	°C/W
Channel Temperature (T_{CH}) (Under RF drive)		130	°C

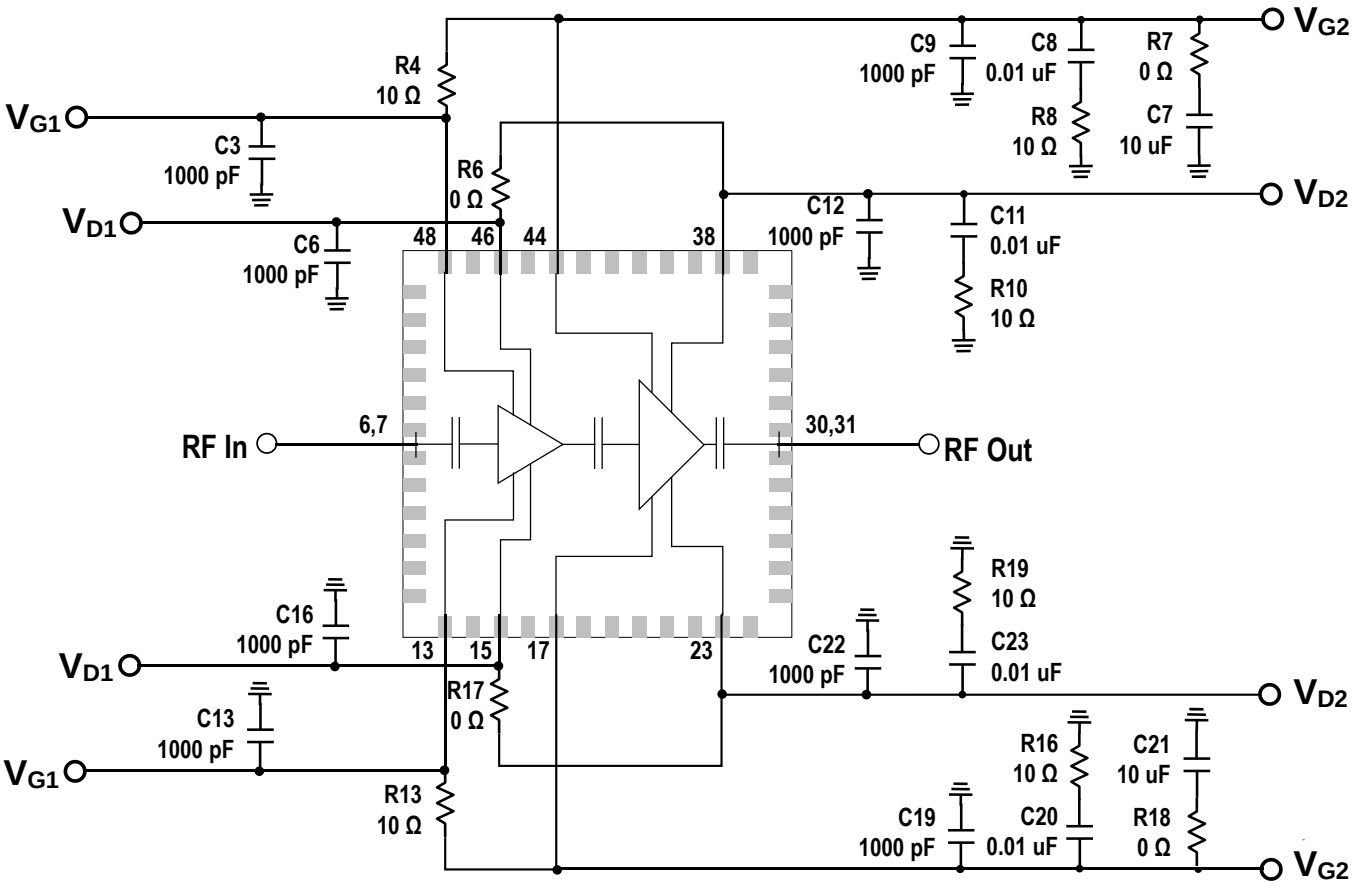
Notes:
1. Thermal resistance is measured to back of package.
2. IR scan equivalent. Refer to the following document: GaN Device Channel Temperature, Thermal Resistance, and Reliability Estimates

Power Dissipation & Maximum Gate Current





Applications Circuit



Notes:

1. V_G and V_D must be biased from both sides (top and bottom).

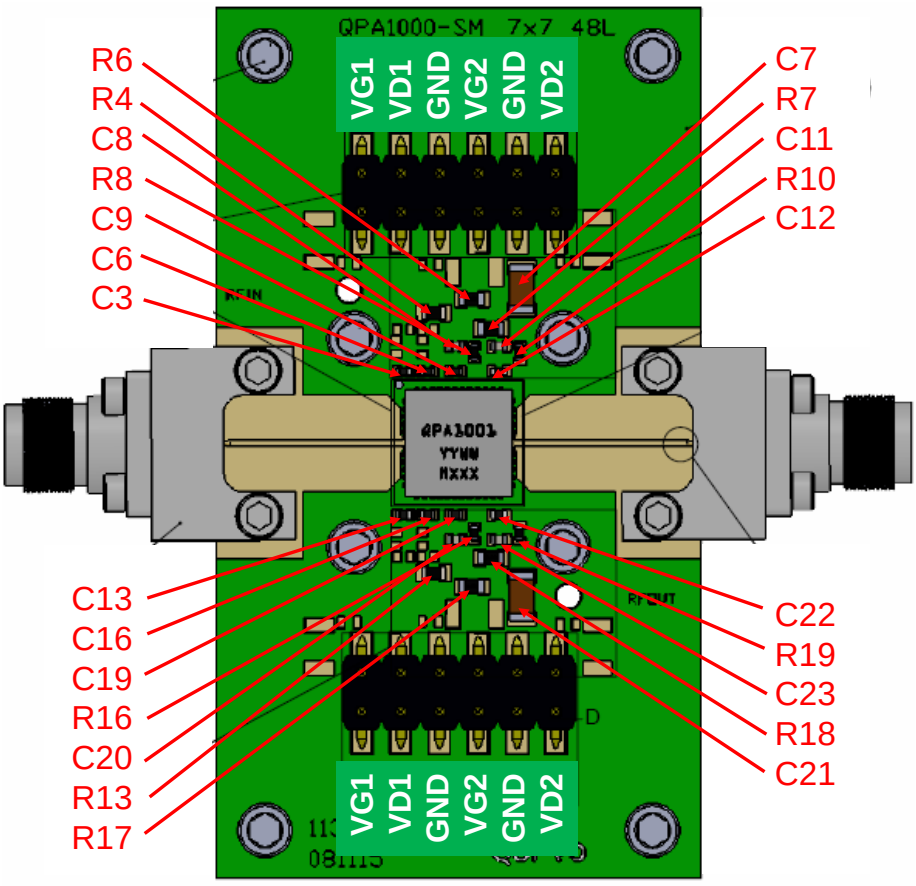
Bias Up Procedure

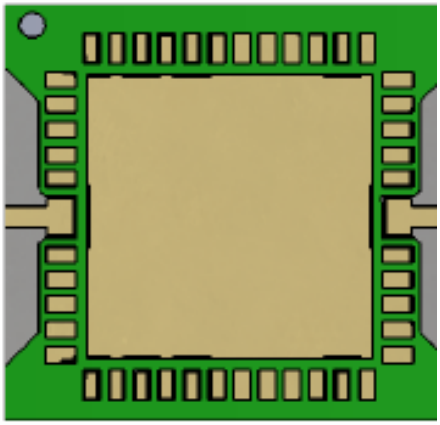
1. Set I_D limit to 6000mA, I_G limit to 40mA
2. Set V_G to −6.0 V
3. Set V_D +25 V
4. Adjust V_G more positive until I_{DQ} = 200mA (V_G ~ −2.8 V Typical)
5. Apply RF signal

Bias Down Procedure

1. Turn off RF supply
2. Reduce V_G to −6.0V. Ensure I_{DQ} ~ 0mA
3. Set V_D to 0 V
4. Turn off V_D supply
5. Turn off V_G supply

Evaluation Board and Mounting Detail





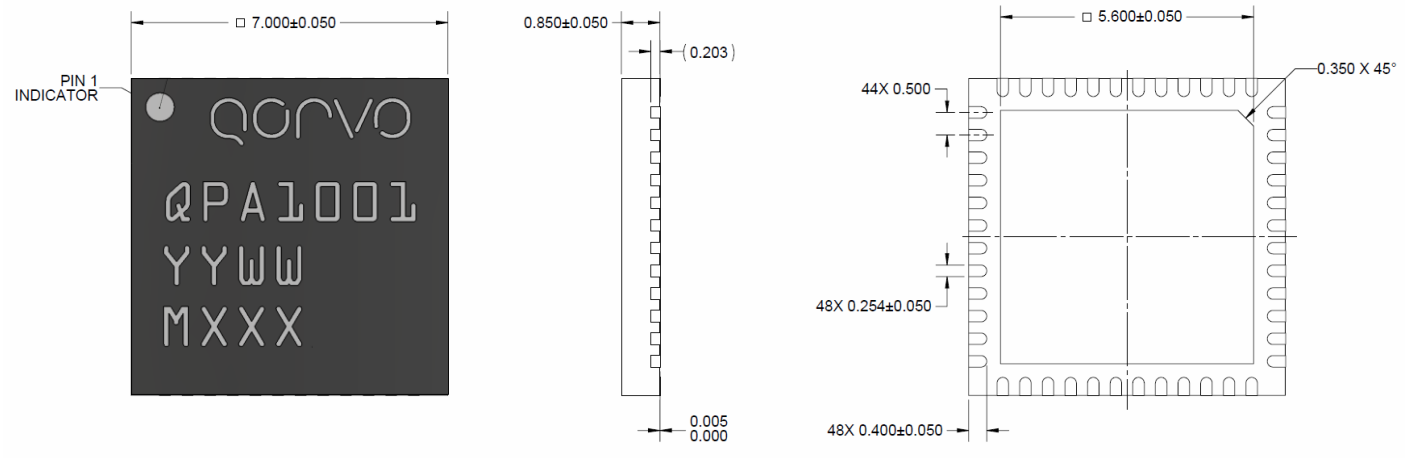
Mounting Detail

RF Layer is 0.008" thick Rogers Corp. RO40003C (εr = 3.35). Metal layers are 0.5 oz. copper. The microstrip line at the connector interface is optimized for the Southwest Microwave end launch connector 1092-02A-5.

Bill of Materials

Ref. Des.	Component	Value	Manuf.	Part Number
C7, C21	Surface Mount Cap.	CAP, 1206, 10uF, 20%, 50V, 20%, X5R	Various	
C3, C6, C9, C12, C13, C16, C19, C22	Surface Mount Cap.	CAP, 0402, 1000pF, 10%, 100V, X7R	Various	
C8, C11, C20, C23	Surface Mount Cap.	CAP, 0402, 0.01uF, ±10%, 50V, X7R	Various	
R8, R10, R16, R19	Surface Mount Res.	RES, 10 OHM ± 5% 0402	Various	
R4, R13	Surface Mount Res.	RES, 10 OHM 1/10W ± 5% 0603	Various	
R6, R7, R16, R18	Surface Mount Res.	RES, 0 OHM 5% 0603	Various	

Mechanical Information



NOTES:
PACKAGE METAL BASE AND LEADS ARE GOLD PLATED.
PART IS PLASTIC MOLD ENCAPSULATED.

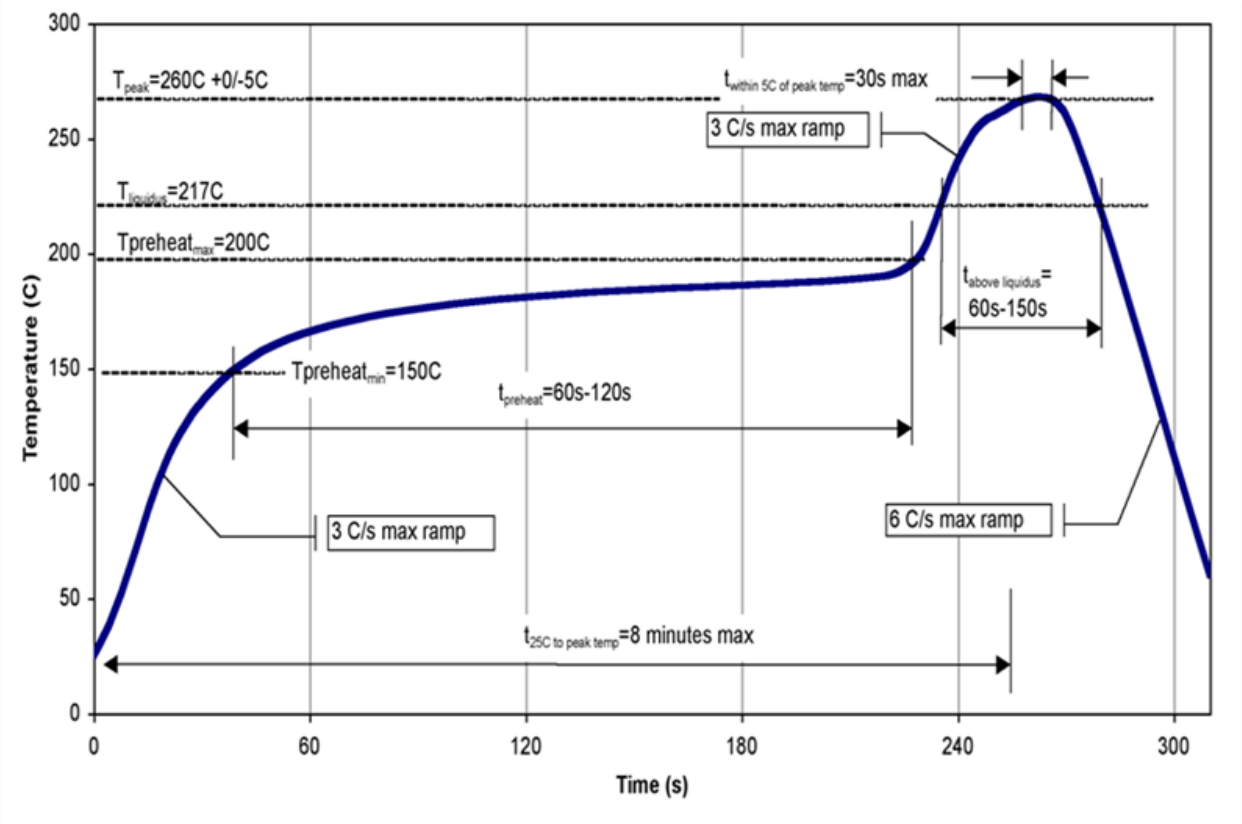
PART MARKING:
QPA1001: PART NUMBER
YY: PART ASSY YEAR
WW: PART ASSY WEEK
MXXX: LOT NUMBER

DIMENSIONS IN MM

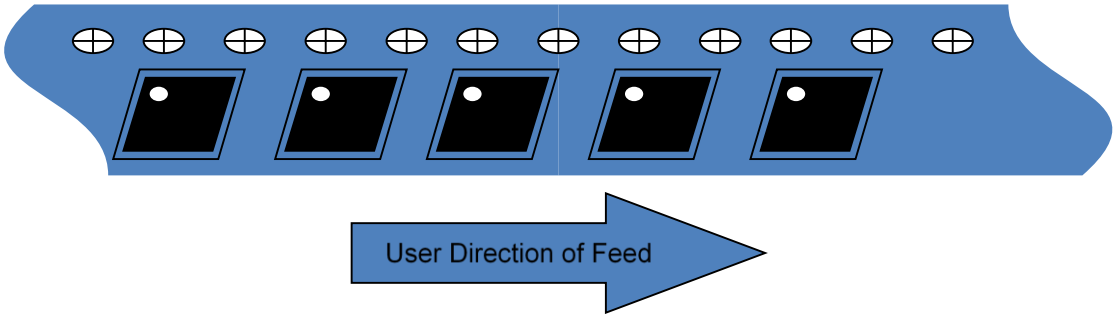
Pin Description

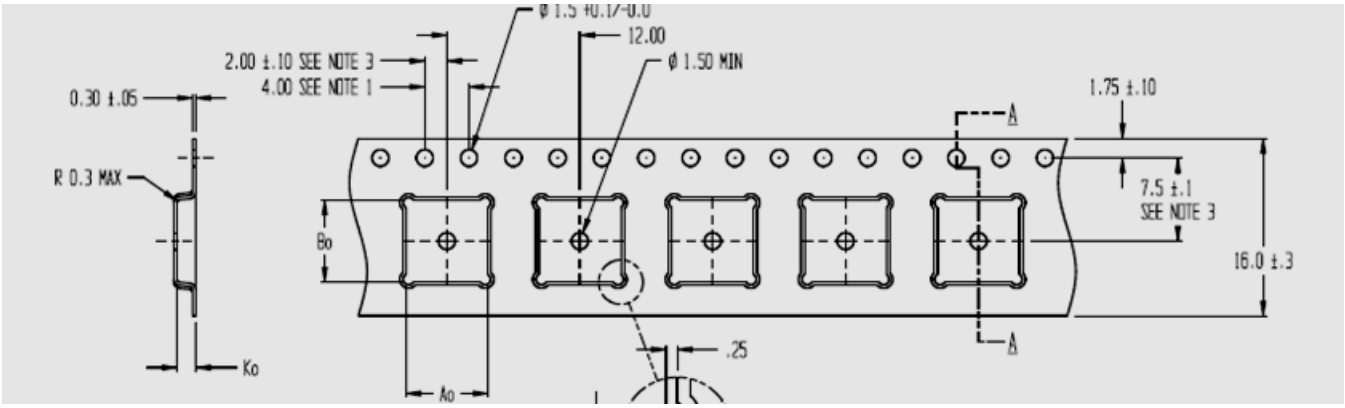
Pin Number	Symbol	Description
1-5, 8-12, 14, 16, 18-22, 24-29, 32-37, 39-43, 45, 47	NC	No connection. Can be grounded on PCB if desired.
6, 7	RF Input	50 Ohm RF input. Pad is capacitively coupled to block on-chip DC voltages.
13, 48	V_{G1}	1st Stage Gate Voltage; bias network is required; must be biased from both sides (V_{G1} and V_{G2} can be tied together in application)
15, 46	V_{D1}	1st Stage Drain Voltage; bias network is required; must be biased from both sides (V_{D1} and V_{D2} can be tied together in application)
17, 44	V_{G2}	2nd Stage Gate Voltage; bias network is required; must be biased from both sides (V_{G1} and V_{G2} can be tied together in application)
23, 38	V_{D2}	2nd Stage Drain Voltage; bias network is required; must be biased from both sides (V_{D1} and V_{D2} can be tied together in application)
30, 31	RF Output	50 Ohm RF output. Pad is capacitively coupled to block on-chip DC voltages.
49 (center pad)	GND	Ground connection.

Recommended Soldering Temperature Profile



Tape and Reel Information – Carrier and Cover Tape Dimensions

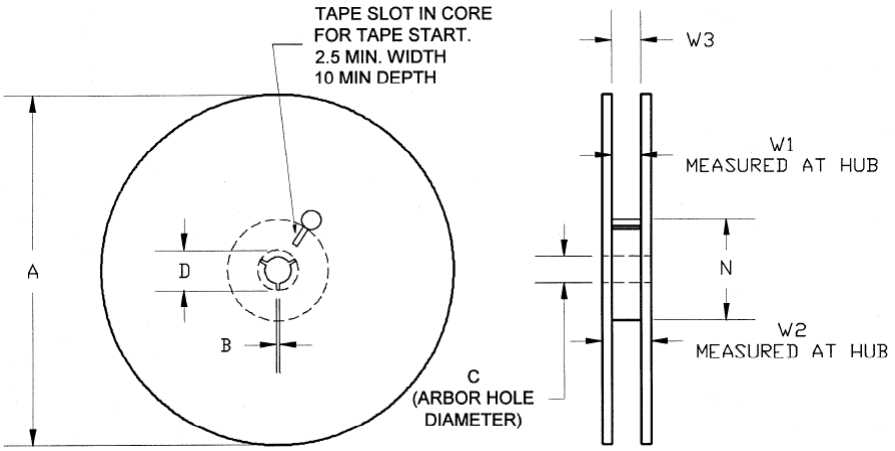




Feature	Measure	Symbol	Size (in)	Size (mm)
Cavity	Length	A0	0.285	7.25
	Width	B0	0.285	7.25
	Depth	K0	0.043	1.10
	Pitch	P1	0.472	12.00
Centerline Distance	Cavity to Perforation - Length Direction	P2	0.078	2.00
	Cavity to Perforation - Width Direction	F	0.295	7.50
Cover Tape	Width	C	0.524	13.3
Carrier Tape	Width	W	0.630	16.0

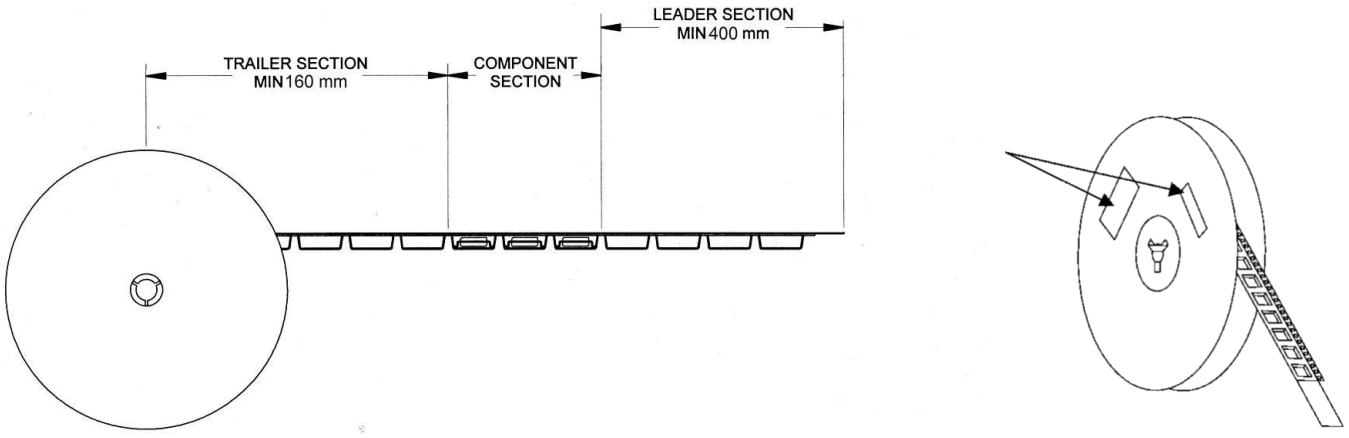
Tape and Reel Information – Reel Dimensions

Standard T/R size = 500 pieces on a 7” reel.



Feature	Measure	Symbol	Size (in)	Size (mm)
Flange	Diameter	A	6.969	177.0
	Thickness	W2	0.874	22.2
	Space Between Flange	W1	0.661	16.8
Hub	Outer Diameter	N	2.283	58.0
	Arbor Hole Diameter	C	0.512	13.0
	Key Slit Width	B	0.079	2.0
	Key Slit Diameter	D	0.787	20.0

Tape and Reel Information – Tape Length and Label Placement



Notes:
1. Empty part cavities at the trailing and leading ends are sealed with cover tape. See EIA 481-1-A.
2. Labels are placed on the flange opposite the sprockets in the carrier tape.